# A LOW NOISE FET AMPLIFIER IN COPLANAR WAVEGUIDE

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## Abstract

This paper describes the factors affecting the performance of low noise FET amplifiers, with particular emphasis on the advantages of coplanar waveguide as the microwave circuit. RF results include overall amplifier noise figures of 2.2 dB at 7.5 GHz from devices made from two quite different GaAs structures.

## Introduction

The factors affecting the performance of FET amplifiers are the characteristics of the semiconductor material, the device technology used, and the properties of the microwave circuit. This paper describes work in these areas directed towards a low noise amplifier operating at 7.5 GHz. The alternative material structures and the device technology used to achieve low noise will be briefly discussed but the main body of the paper will describe the use of coplanar waveguide in the design and construction of the complete amplifier module. The particular advantages of this transmission medium will be discussed and some amplifier results presented.

## Semiconductor Material Characteristics

GaAs is the material used as it appears to offer, at the moment, the best combination of electrical properties, contacting technology and availability of high quality multiple sub-micron active layers and buffer layers. Three types of growth structures, as shown in Figure 1, have been tried: $n^+$ on n on semi-insulating (SI) substrates grown by Molecular Beam Epitaxy, n on high resistivity buffer layer on SI substrates grown by $AsCl_3$ vapour phase epitaxy (VPE), and $n^+$ on n on thin p buffer on SI substrates grown by alkyl VPE[1]. RF results achieved are consistent with the view that good performance can only be obtained from structures that have a high quality buffer layer between the SI substrate and the active layer.

## Device Technology

Hewitt et al[2] have developed an expression for the noise of an FET which indicates that the minimum noise temperature is approximately proportional to the gate length multiplied by the square root of the sum of the parasitic resistances (source resistance plus gate metallisation resistance). Gates, with dimensions in the range 0.5 - 1.0 μm long, have been made using electron lithography to define the electrode patterns. Low source resistances have been achieved by the combination of thick semiconductor material under the source pad and a low RF specific contact resistance between the In Ge Au metallisation and the GaAs. Low resistances have resulted from using two, and in some instances, four gates connected in parallel, and by developing techniques for floating off gold films up to 1.5 μm thick. A cross section of a typical device is shown in Figure 2.

## Microwave Circuit

In general, and particularly at higher frequencies, optimum amplifier RF performance can only be achieved if the parasitic reactances associated with mounting the device in the microwave circuit are minimised and if there is some degree of tuneability in the matching arrangements. As an FET is a planar device, the mounting parasitics can be minimised by flip-chipping the device directly onto a planar circuit, for example, coplanar waveguide[3] (CPW). This particular circuit has the considerable advantage that both series and shunt elements can very easily be added to it; series elements by making a break in the centre conductor, and shunt elements by connecting directly between the centre conductor and the adjacent ground planes. Figure 3 illustrates how a double FET design, in common source configuration, is flip-chipped onto CPW. Common gate connections have also been made using different chip metallisation patterns.

Devices can be tuned over a wide frequency range by placing anodised aluminium plates across the circuit on both input and output as shown in Figure 3. The magnitude of the tuning impedance can be adjusted by selecting tuners of differing lengths and thicknesses of insulation, and the phase adjusted by moving the tuners along the CPW. By this means devices have been tuned for either minimum noise or maximum gain, or intermediate performance between these extremes, without prior knowledge of the RF characteristics of the chip.

After the tuners have been optimised in position, they are clamped in place by means of a simple jig, forming a rugged circuit. Typical single stage bandwidths are of the order of 5% to 10%, but bandwidths approximately double these figures have been achieved by using a second tuner on the output. Transitions to both coax and waveguide, and with appropriate bias arrangements, have been readily made with VSWR's of better than 1.1 over 15% bandwidth. Figure 4 is a photograph of a coplanar waveguide circuit with bias inputs at either end. The transitions to coax or waveguide are made at the annular areas one fifth of the way in from either end.

Devices with more than two gates in parallel can also be flip chipped onto CPW. For example, four gate devices have been mounted in this manner in common source configuration. The gates were joined together on the chip but the three sources were connected by a metal stripe running along indentations in the CPW dielectric substrate and which joined the two ground planes in the gap between the centre conductors.

## RF Amplifier Results

Using the techniques described, 0.8 μm gate length devices made from both the alkyl and the commercially grown $AsCl_3$ VPE material have been operated in CPW circuits at 7.5 GHz and have given virtually identical noise results. Figure 5 is a graph of noise figure vs associated gain for complete single stage amplifiers (i.e. from APC-7 input to APC-7 output) at 7.5 GHz. Any one curve is the set of results for one amplifier under a variety of tuning conditions, and the three curves correspond to chips taken from three different slices, two alkyl and one $AsCl_3$ grown VPE. As can be seen, amplifier minimum noise figures of 2.2 dB have been achieved from chips made from GaAs slices with two quite different epitaxial structures. The minimum amplifier noise

figures correspond to chip noise figures of about 1.8dB. The corresponding best chip noise figure on the unbuffered MBE material was about 3.3 dB.

## Conclusions

Low noise FET amplifiers have been made using chips fabricated from two quite different GaAs epitaxial structures. Parasitic reactances were minimised by flip-chipping the devices directly onto coplanar waveguide. Simple anodised aluminium plates served as wide range and easily varied tuners, permitting optimum performance to be achieved from a given device without prior knowledge of the RF characteristics of the chip.


## Acknowledgements

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## References


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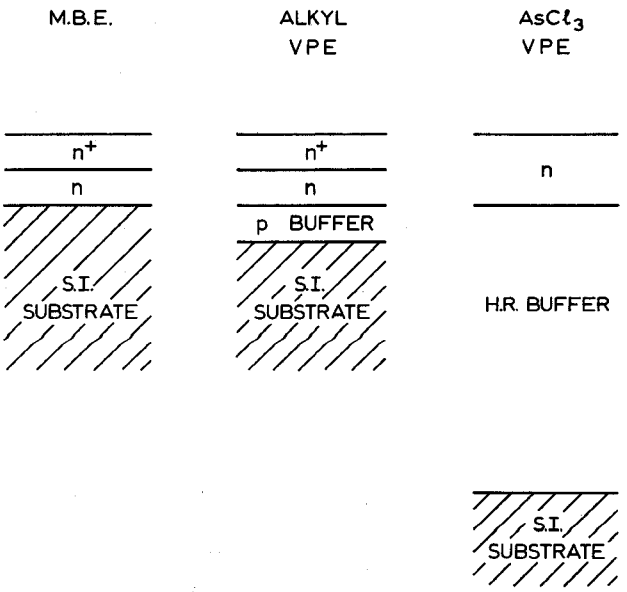


Figure 1. GaAs epitaxial growth structures.

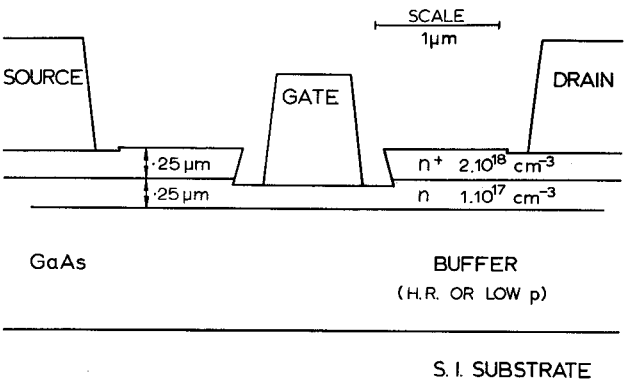


Figure 2. Cross section of active region of typical FET.

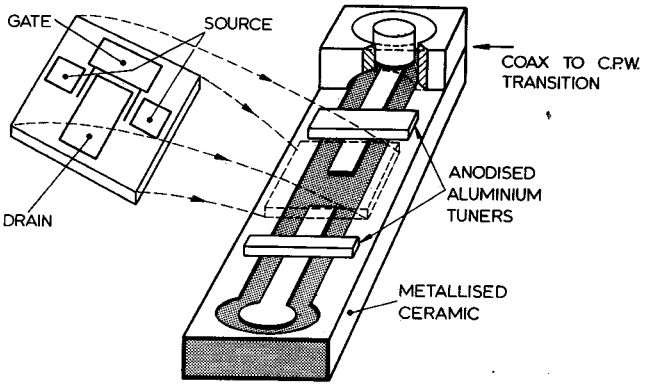


Figure 3. Schematic view of chip and coplanar waveguide circuit.

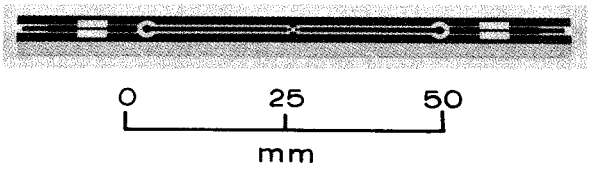


Figure 4. Coplanar waveguide circuit.

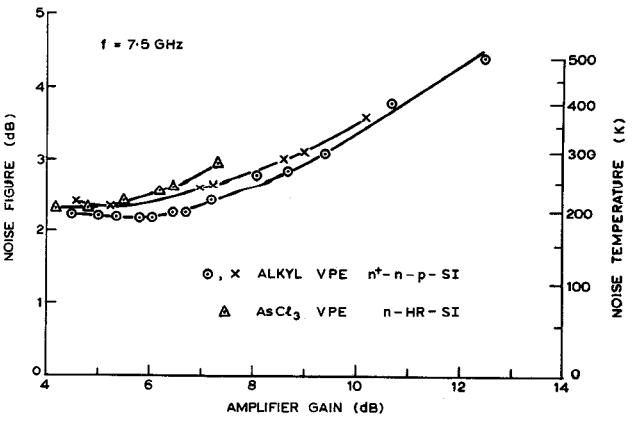


Figure 5. Single stage amplifier results for three devices, each from a different slice.